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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,970	10/29/2003	Shay Ben-David	IL920030035US1	7994

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EXAMINER	
STEELMAN, MARY J	
ART UNIT	**PAPER NUMBER**
2191	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,970	BEN-DAVID ET AL.	
	Examiner	Art Unit	
	Mary J. Steelman	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/29/2003,4/1/04,12/6/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/6/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 are pending.

Drawings

2. FIG 2D, received 04/01/2004, does not comply as it fails to state "Replacement Sheet".

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:
FIGs 1A & 1B are missing #100 through #112. Additionally the number of bits shown in the drawing are confusing.

FIG. 5C is missing a description for #514 & #516 in the Specification (p. 11).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

4. IDS received 12/06/2005 has been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-7, 9-18, 20-29, and 31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by U S Patent Application Publication 2005/0055536 A1 to Ansari.

Per claims 1, 12, and 23:

A method for determining vectorization configurations in a computer processor architecture, the method comprising:

-identifying a vectorizable loop in a computer program; identifying a memory access pattern of data required for implementing said loop in said architecture;

Ansari: [0061] compiler looks for loops, candidate loops include...constant stride and offset, including a larger loop trip count (memory access patterns).

-computing a set of candidate configuration s of resources required for vectorizing said data in said architecture, wherein said computing step comprises configuring a vector pointer register of said architecture in support of either of reorder-on-read use and reorder-on-write use of a vector element file of said architecture;

Ansari: [0064-0067], vector instructions, [0077], vector store instruction, [0117] Rx, Rt are registers, [0088], the entry point in the vector buffer pointed to by the contents of register Rs is loaded into the Rt register.

-selecting one of said candidates in accordance with predefined selection criteria;

Ansari: [0117], compiler allocates one or more buffers to each program and partitions each buffer into variable sized vector streams.

-implementing said selected vectorization configuration in said architecture.

Ansari: [0117], partitions buffer.

Per claims 2, 13, and 24:

-any of said steps are implemented by a compiler.

Ansari: [0117], compiler

Per claims 3, 14, and 25:

-said computing step comprises configuring any of said vector pointer registers in support of loading a data vector into a plurality of non-contiguous segments of said vector element file of said architecture.

Ansari: [0122], load instruction, [0143], allocate buffers.

Per claims 4, 15, and 26:

-said computing step comprises configuring any of said vector pointer registers in support of loading a data vector into said vector element file of said architecture in support of a

plurality of operations where each operation has a different access pattern.

Ansari: [0122], integer & float operations (plurality of operations), [0143], different bit combinations specify different buffer size. See claim 1 regarding register usage and claim 3 regarding vector load instructions.

Per claims 5, 16, and 27:

-performing any of said steps for a plurality of vectorizable loops in the same computer program;

Ansari: [0061], loops

-detecting a data reuse opportunity common to two or more of said loops;

Ansari: [0062], vector data used by each iteration, [0118[, accelerate using single port SRAM, programs requiring a contiguous vector buffer for doing multilevel loop nests, data reuse, and data manipulation.

-modifying any of said candidate configuration in support of said data reuse opportunity.

Ansari: [0124], compiler code relocation, [0117] partition buffer into variable sized vector streams.

Per claims 6, 17, and 28:

-eliminating any of said candidates in accordance with predefined elimination criteria.

Ansari: [0128-0130], Kernel can overwrite and empty.

Per claims 7, 18, and 29:

-said eliminating step comprises eliminating any of said candidates that requires loading a data vector into said vector element file in a manner that cannot be accommodated by said vector element file.

Ansari: [0076], [0125], candidate stream may not exceed page boundary.

Per claims 9, 20, and 31:

A method for determining vectorization configurations in a computer processor architecture for computations that feature arbitrary parametric access, the method comprising:

-identifying a loop in a computer program that accesses data indirectly;

Ansari: [0013],

-determining that indices of said loop fit within the range of a vector element file of said architecture,

Ansari: [0076]

-and, if so:

-loading all loop data into said vector element file;

Ansari: [0063-0088], loading instructions

-loading said indices into at least one vector pointer register of said architecture in support of reorder-on-read use of said vector element file;

Ansari: See claim 1 above regarding vector registers (Rs), indices are loaded into register from memory access (reorder on read use).

-vectorizing said loop data.

Ansari: [0088]

Per claims 10, 21, and 32:

-said identifying step comprises identifying said loop as performing a plurality of computations that operate in parallel on a permutation of data.

Ansari: [0017], synchronization instruction

Per claims 11, 22, and 33:

-where any of said steps are implemented by a compiler.

Ansari: [0063+]

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8, 19, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U S Patent Application Publication 2005/0055536 A1 to Ansari, in view of US Patent 6,446,105 B1 to Washio et al.

Per claims 8, 19, and 30:

-said selecting step comprises selecting one of said candidate configurations that uses fewest vector pointer registers among all of said candidates.

Ansari failed to disclose a register optimization option.

However, Washio disclosed (col. 9: 33-39) consideration to the queue length and the number of memory banks, so that the vector process more rapidly. Col. 7: 48-52, processing of the commands is distributed over a plurality of independent vector processors operating in parallel. Col. 7: 65-66, the actual vector length is greater than that for the minimum vector length. Col. 8:5-8, Rules ensure that all calculating operations can be executed independently of one another within a color subset, so that vector processing becomes possible within a color subset (optimal number of registers allocated).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Ansari, using the teachings of Washio because Ansari recognized the need to handle large amounts of data such as [0010] multi-media vector data efficiently. Ansari's compiler effectively synchronizes the data and an optimal register allocation improves the efficiency.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached at (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned: 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

02/06/2007